Gate oxide degradation of SiC IGBT induced by non-constant thermal-electrical coupled stresses

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Introduction

Silicon carbide (SiC) is a wide band gap material with excellent thermal conductivity and a high breakdown electric field. It is a candidate material for high-power and high-frequency electronic devices. However, the imperfections of the fabrication process cause the SiC/SiO_2 interface properties of SiC IGBTs to be poorer than the Si/SiO_2 interface of Si IGBTs, which has become a non-negligible reliability risk for SiC power electronic devices. The degradation mechanism of the SiC/SiO_2 interface of SiC IGBTs under non-constant thermal-electrical coupled stresses was investigated in this study, based on variation analysis of sensitive static characteristics. Under positive bias (Group 2: +70 V, Group 3: +50 V) at 150 ℃ for 675 h, $V_{GE(TH)}$ increased slightly. Then a mild rebound happened to Groups 2 and 3 after 15 days of recovery (Stage 2: under 25 ℃ / 50 %RH). Afterwards, a significant decrease of $V_{GE(TH)}$ within 48 h under negative bias (Group 2: -70 V, Group 3: -50 V), probably due to the holes captured by traps rapidly at or near the SiC/SiO_2 interface. The harsher stresses led to more serious $V_{GE(TH)}$ drift as expected. While no significant $V_{GE(TH)}$ fluctuations were observed after HTSS tests (at 150 ℃). Besides, the I_{GES} and $V_{(BR)CES}$ did not change significantly, which indicates there is no permanent damage.

Experimental methods

DUTs of Group 1 were exposed to **constant thermal stress** only, for comparison to Group 2 and Group 3. The DUTs of Group 2 and Group 3 were exposed to **non-constant thermal-electrical coupled stresses**, more specifically, the progress of the tests included 675h of HTGB test under positive gate bias (**Stage 1**, Group 2: +70 V, Group 3: +50 V), 15 days of recovery under 25 ℃/50 %RH (**Stage 2**), and 430h of HTGB test under negative gate bias (**Stage 3**, Group 2: -70 V, Group 3: -50 V), the thermal-electrical coupled stresses profile can be seen in **Figure. 1**, with the high temperature gate bias **(HTGB**) and high temperature storage stress **(HTSS**) tests condition clarified.

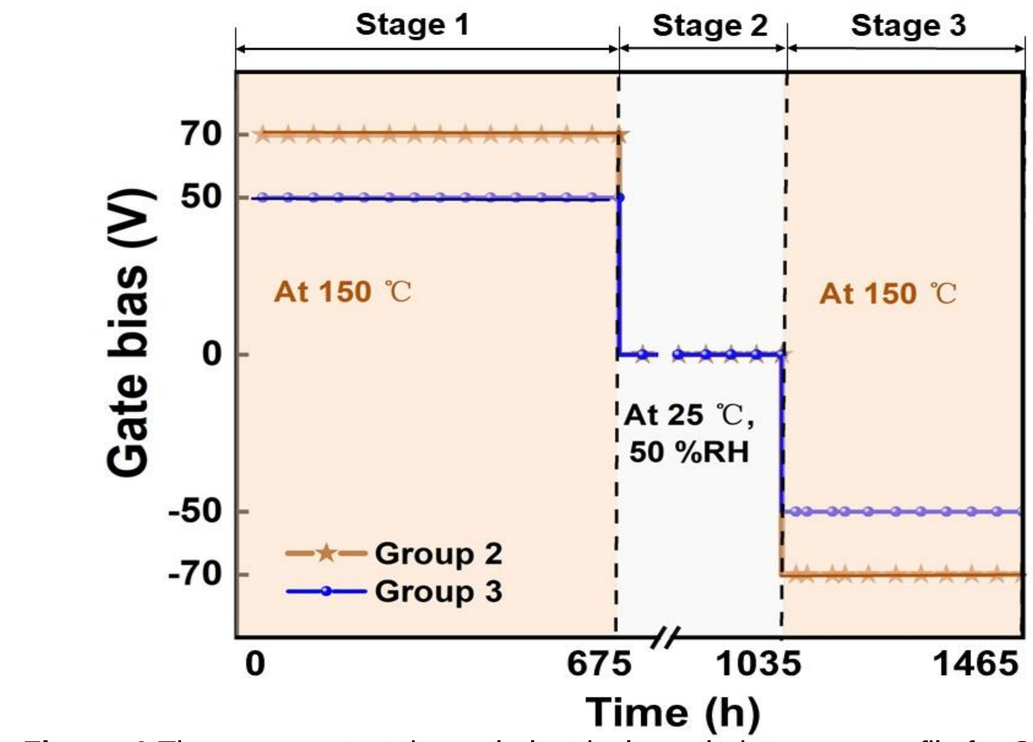

Figure. 1 The non-constant thermal-electrical coupled stresses profile for Group 2 and Group 3

The variation of the $V_{GE(TH)}$

The variation of $V_{GE(TH)}$, and the change of the average $V_{GE(TH)}$ ($\Delta V_{GE(TH)}$) over time for Group 1 are shown in **Figure**. 2. After the HTSS tests (1100 h), $V_{GE(TH)}$ decreased slightly, with an average $V_{GE(TH)}$ of 5.334 V, a change of only **-0.726%**. The average change of $V_{GE(TH)}$ ($\Delta V_{GE(TH)}$) during the overall tests period for Groups 2 and 3 is displayed in **Figure**. 3. The $V_{GE(TH)}$ of Group 2 and Group 3 changed by **2.37%** and **0.68%**, respectively, after the positively biased HTGB tests (Stage 1). When a negative bias is applied (Stage 3), the $V_{GE(TH)}$ decreases. The drifts in $V_{GE(TH)}$ under negative gate bias stress are significantly larger than those under positive, and the average variations ($\Delta V_{GE(TH)}$) of Groups 2 and Group 3 are **-8.89%** and **-6.21%,** respectively.

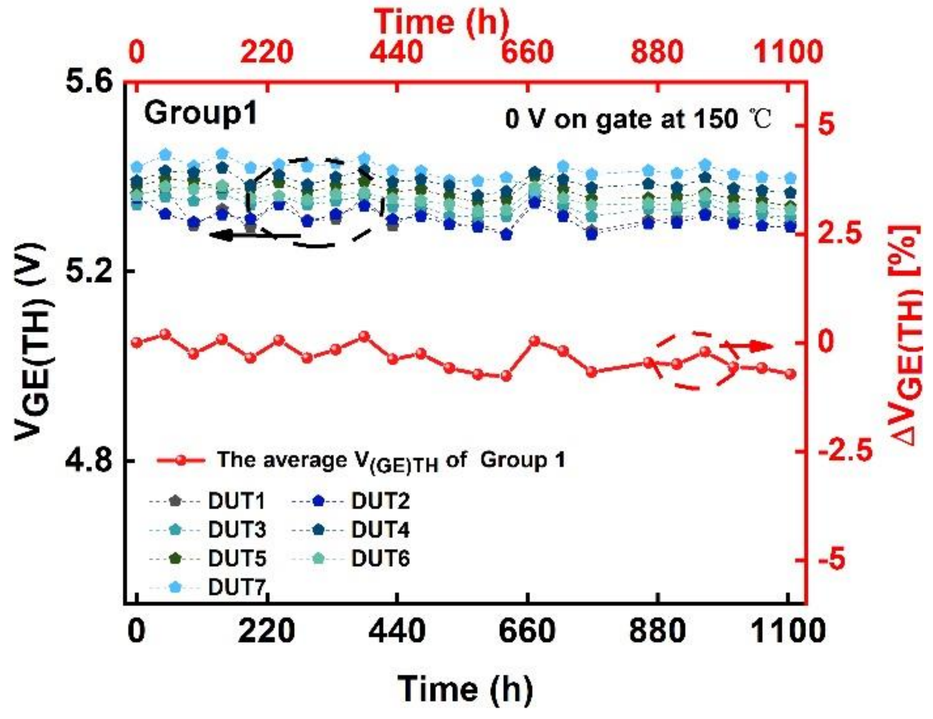

Figure. 2 The $V_{GE(TH)}$ and the average $V_{GE(TH)}$ change ($\Delta V_{GE(TH)}$) of Group 1 as a function of time under constant temperature (150 ℃)

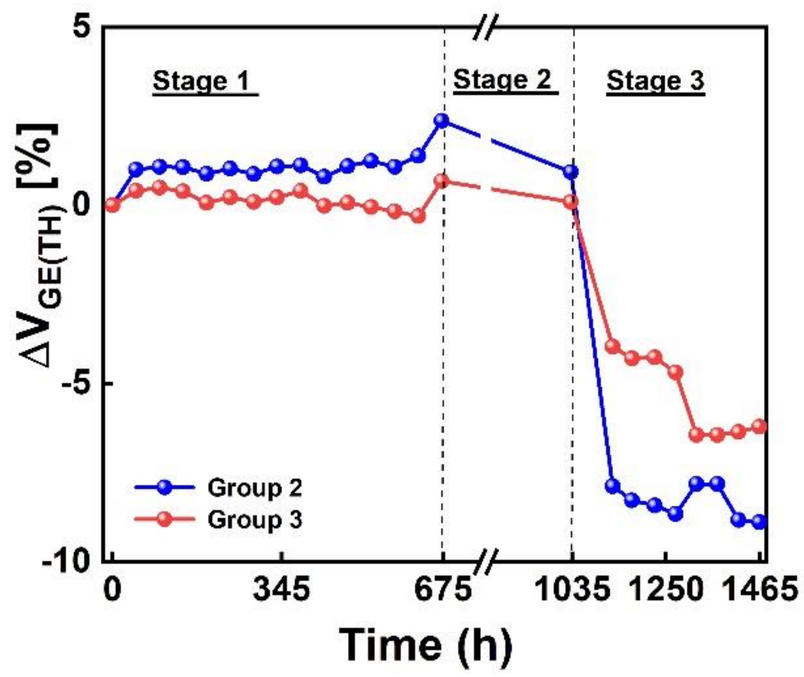

Figure. 3 Measured changes of the average $V_{GE(TH)}$ ($\Delta V_{GE(TH)}$) of Group 2 & Group 3

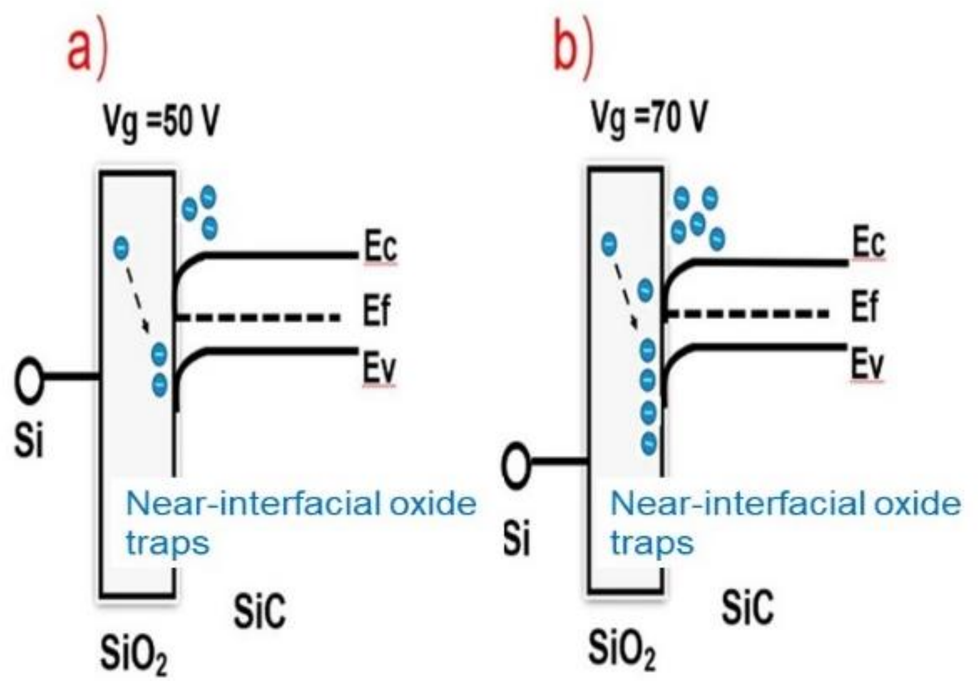

Figure. 4 Energy band diagrams for the DUTs under two positive gate bias stresses: a) Vg=50 V and b) Vg=70 V

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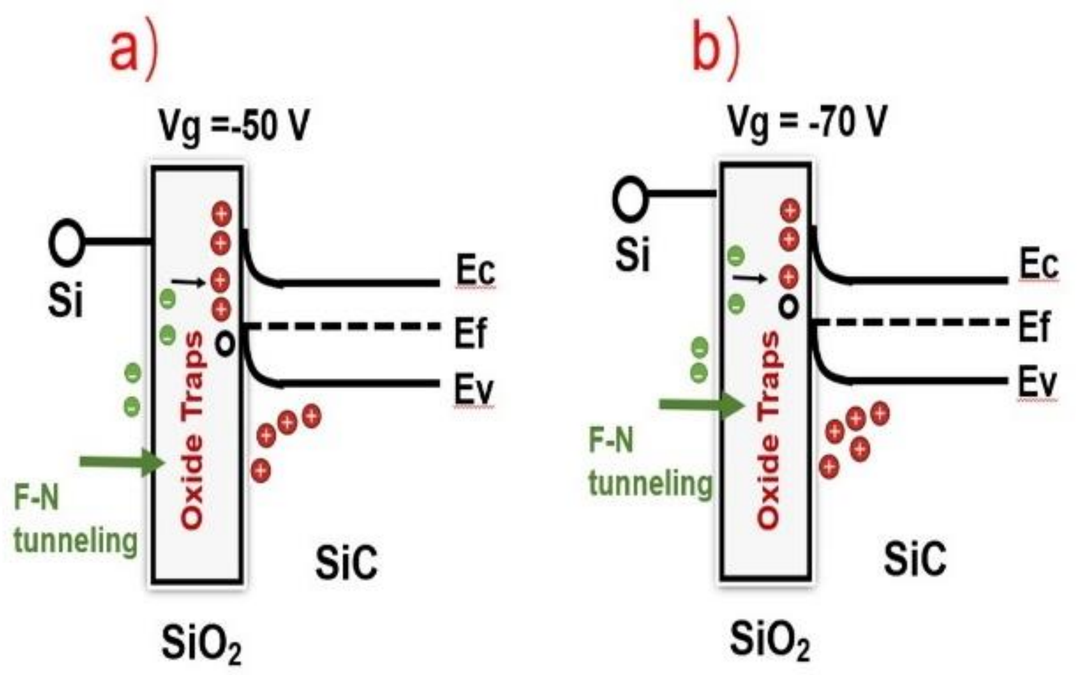


Figure. 5 Energy band diagrams for the DUTs under two negative gate bias stresses: a) Vg=-50 V, b) Vg=-70 V

The energy band diagram of the gate region

The energy band diagram of the gate region can explain the $V_{GE(TH)}$ instability during HTGB tests. As shown in **Figure. 4**, when a positive gate voltage is applied, which indicates the formation of **an electron-stacking region** in the semiconductor. Under thermal-electrical coupled stresses, electrons are trapped by the near-interfacial oxide traps at or near the SiC/SiO_2 interface. The electron trapping capability **increases** with increasing gate voltage.

As shown in **Figure. 5**, when a negative gate voltage is applied, the holes are trapped by the hole traps , indicating the formation of a **hole-stacking region** in the semiconductor. As the negative gate voltage increases, the number of trapped holes will result in a negative drift of the threshold voltage. In addition, we can see that the threshold voltages of the two groups showed a transient positive offset (Group 2 at 1008 h, Group 3 at 1056 h and 1465 h), which may be due to the **Fowler-Northeim (F-N) tunnelling mechanism** causing additional electrons to cross the gate oxide , creating new electron traps and elevating $V_{GE(TH)}$. It is also possible that the $V_{GE(TH)}$ increases due to the generation of new electron traps during the test.

The variation of the I_{GES} and the $V_{(BR)CES}$

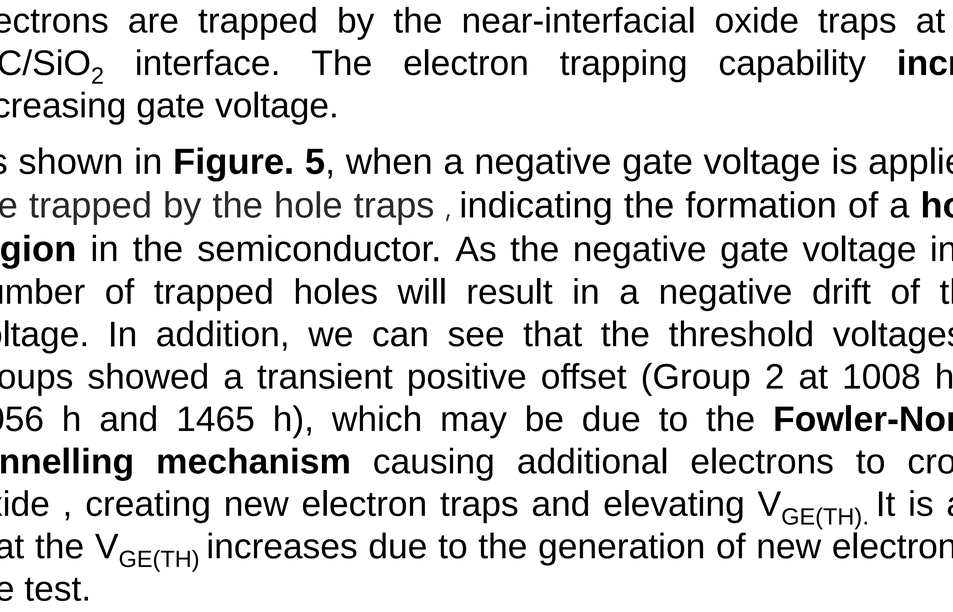
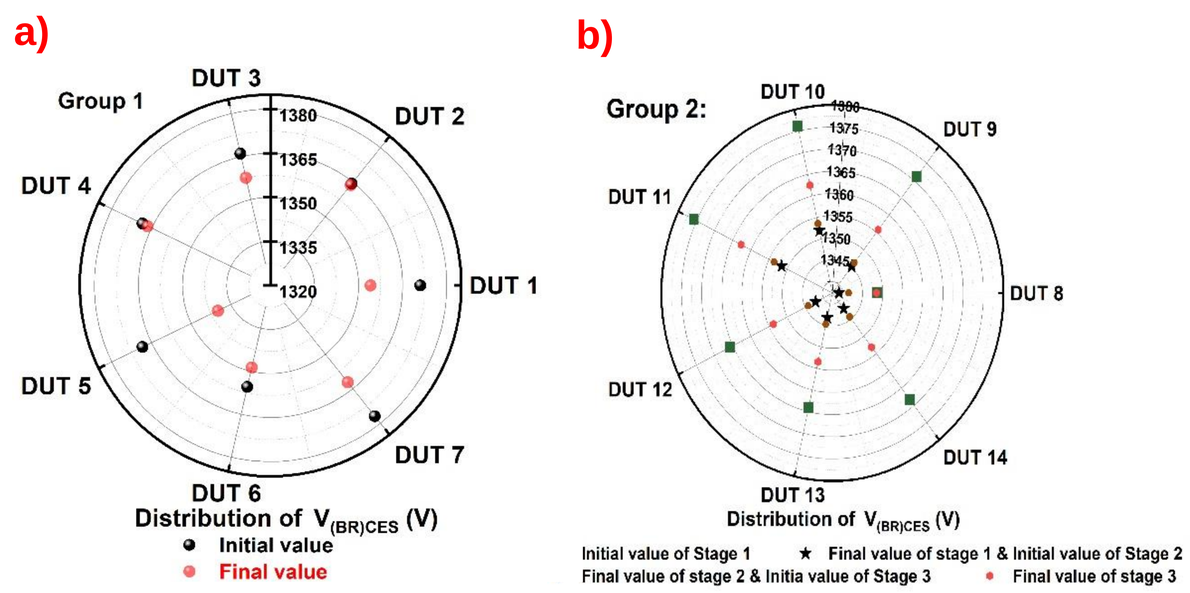


Figure. 6 Comparison of the average I_{GES} among the three groups before and after tests

The variation of the $V_{(BR)CES}$



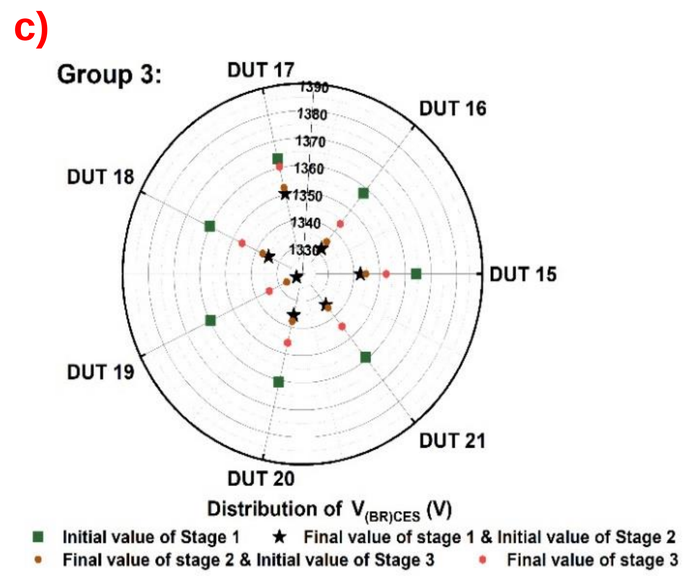


Figure. 7 The $V_{(BR)CES}$ distribution of each device in Group 1 to 3 before and after the test: a) Group 1, b) Group 2, c) Group 3.

Conclusion

This paper evaluated the **SiC/SiO_2 interface** property of commercial SiC IGBTs under non-constant thermal-electrical coupled stresses, based on the variation trends of sensitive static characteristics, i.e., gate threshold voltage ($V_{GE(TH)}$), gate-emitter leakage current (I_{GES}), and collector-emitter breakdown voltage ($V_{(BR)CES}$).

The $V_{GE(TH)}$ increased slightly (within 675 h of HTGB tests, at 150 ℃) under positive bias voltages (Group 2: +70 V and Group 3: +50 V). When it came to a recovery stage of 15 days (last for 360 h, at 25℃, 50 %RH), the $V_{GE(TH)}$ had a small rebound because the gate oxide internal charge and interface trap density decreased. Afterwards, switching the bias voltage to -70 V and -50 V for Group 2 and Group 3 (Stage 3, at 150 ℃), the $V_{GE(TH)}$ dramatically dropped, with corresponding average variations ($\Delta V_{GE(TH)}$) of -8.89% and -6.21%, respectively. **It can be attributed to holes captured by the traps at or near the SiC/SiO_2 interface. As expected, the harsher thermal-electrical coupled stresses led to more serious degradation of the SiC/SiO_2 interface property (Group 2).** Note that, the constant thermal stress (HTSS test) resulted in an almost unchanged $V_{GE(TH)}$ for Group 1.

In addition, either the increase of leakage current (always with a magnitude of pA) or the decrease of breakdown voltage can be ignored for SiC IGBTs in this study, indicating no permanent damage existing after the accelerated tests.